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L2: Entry 1 of 4

File: USPT

Dec 21, 1999

US-PAT-NO: 6006033

DOCUMENT-IDENTIFIER: US 6006033 A

TITLE: Method and system for reordering the instructions of a computer program to optimize its execution

DATE-ISSUED: December 21, 1999

## INVENTOR-INFORMATION:

| NAME                | CITY   | STATE | ZIP CODE | COUNTRY |
|---------------------|--------|-------|----------|---------|
| Heisch; Randall Ray | Austin | TX    |          |         |

US-CL-CURRENT: 717/158; 711/125, 711/134

## ABSTRACT:

A system and method are provided that allows the results of an instruction trace mechanism to globally restructure the instructions. The process reorders the instructions in an executable program, using an actual execution profile (or instruction address trace) for a selected workload, to improve utilization of the existing hardware architecture. The reordering of instructions is implemented at a global level (i.e., independent of procedure or other structural boundaries which maximizes speedup) running on various hardware platforms and adds the ability to preserve correctness and debuggability for reordered executables. An unconditional branch instruction is added at the memory locations where reordered instructions previously were stored. When a dynamic branch occurs, the program will attempt to access the instruction at the original address and the unconditional branch directs the program to the reordered location of the instruction and program integrity is maintained.

9 Claims, 16 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 11

|      |       |          |       |        |                |      |           |           |             |        |      |           |       |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|-----------|-------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image |
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☒ 2. Document ID: US 5774724 A

L2: Entry 2 of 4

File: USPT

Jun 30, 1998

US-PAT-NO: 5774724

DOCUMENT-IDENTIFIER: US 5774724 A

TITLE: System and method for acquiring high granularity performance data in a computer system

DATE-ISSUED: June 30, 1998

## INVENTOR - INFORMATION:

| NAME                        | CITY       | STATE | ZIP CODE | COUNTRY |
|-----------------------------|------------|-------|----------|---------|
| <u>Heisch</u> ; Randall Ray | Georgetown | TX    |          |         |

US-CL-CURRENT: 717/129

## ABSTRACT:

A microprocessor performance monitor and instruction address break point facility are interconnected to provide finer granularity and performance monitoring. The microprocessor is initialized to collect processor statistics preselected prior to performance monitoring. Application start and stop instruction breakpoint addresses are preselected from a software program bounding instructions for which such statistics are desired. An exception handler is installed for instruction address breakpoints (IAB), enabling and disabling the performance monitor and stop addresses, respectively. The IAB register is then initialized to the start address, and the statistics counters are cleared. Upon starting the application, when the application start address instruction is executed, the breakpoint handler obtains control and enables the performance monitor counters, which count the desired statistics after returning from the breakpoint handler. Before returning, the handler sets the IAB register to the stop address. When the application stop address is encountered, the breakpoint handler disables the performance monitor counters, and rearms the start address in the IAB register. The performance monitor counters are then read to determine the desired statistics for the specific sequence of code within the boundaries of the start and stop addresses in the application.

27 Claims, 3 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

|      |       |          |       |        |                |      |           |           |             |        |     |           |       |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|-----|-----------|-------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KMC | Draw Desc | Image |
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☒ 3. Document ID: US 5613118 A

L2: Entry 3 of 4

File: USPT

Mar 18, 1997

US-PAT-NO: 5613118

DOCUMENT-IDENTIFIER: US 5613118 A

TITLE: Profile-based preprocessor for optimizing programs

DATE-ISSUED: March 18, 1997

## INVENTOR - INFORMATION:

| NAME                       | CITY   | STATE | ZIP CODE | COUNTRY |
|----------------------------|--------|-------|----------|---------|
| <u>Heisch</u> ; Randall R. | Austin | TX    |          |         |
| Kilpatrick; Paul J.        | Austin | TX    |          |         |

US-CL-CURRENT: 717/158

## ABSTRACT:

The present invention is an system and method for optimizing a program, having qualified elements, at the source level. The method includes the steps of instrumenting each path of the qualified elements to create an instrumented program, executing the instrumented program to produce instrumentation information for each of the paths, analyzing the instrumentation information, and in response to the analyzing step, restructuring the program to create an optimize program.

1 Claims, 6 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image |
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☒ 4. Document ID: US 5212794 A

L2: Entry 4 of 4

File: USPT

May 18, 1993

US-PAT-NO: 5212794

DOCUMENT-IDENTIFIER: US 5212794 A

TITLE: Method for optimizing computer code to provide more efficient execution on computers having cache memories

DATE-ISSUED: May 18, 1993

## INVENTOR-INFORMATION:

| NAME                    | CITY        | STATE | ZIP CODE | COUNTRY |
|-------------------------|-------------|-------|----------|---------|
| <u>Pettis</u> ; Karl W. | San Jose    | CA    |          |         |
| Hansen; Robert C.       | Santa Clara | CA    |          |         |

US-CL-CURRENT: 717/153; 714/38

## ABSTRACT:

The method uses statistical information obtained by running the computer code with test data to determine a new ordering for the code blocks. The new order places code blocks that are often executed after one another close to one another in the computer's memory. The method first generates chains of basic blocks, and then merges the chains. Finally, basic blocks that were not executed by the test data that was used to generate the statistical information are moved to a distant location to allow the blocks that were used to be more closely grouped together.

6 Claims, 7 Drawing figures

Exemplary Claim Number: 1,5

Number of Drawing Sheets: 5

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |
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| KWIC | Draw Desc | Image |
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| <a href="#">L3</a> | L1 AND profile            | 17     | <a href="#">L3</a> |
| <a href="#">L2</a> | L1 ADN profile            | 240578 | <a href="#">L2</a> |
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| L3 and (runtime or run ADJ time) | 7         |

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| <u>L1</u> | ((717/153)!.CCLS. )              | 85  | <u>L1</u> |

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